

4 CPU (μ PD78C10G) PIN FUNCTIONS

Pin No.	Terminal	Signal	In/Out	Function
59 64 1 2 3	PA0 PA5 PA6 PA7 PB0	SW1 SW9	In	Inputs from the DIP switches
4	PB1	S1	In	Low when mode switch is "GUITAR"
5	PB2	S2	In	Low when octave switch is "UP"
6	PB3	S3	In	Low when octave switch is "DOWN"
7	PB4	S4	In	Low when mode switch is "PROGRAM"
8	PB5	S5	In	Low when mode switch is "BEND"
9	PB6	LD3	Out	b LED drive signal. Low active.
10	PB7	LD2	Out	# LED drive signal. Low active.
11	PC0	M1	Out	MIDI data output
12	PC1	LD1	Out	Pilot lamp drive signal. Low active.
13	PC2	-	In	2M Hz MIDI clock pulse input
14	PC3	CLR	Out	Resets gate array's built-in counters
15	PC4	CLK	Out	Clock signal for gate array's built-in counter
16	PC5	-	-	Not used
17	PC6	-	In	The guitar becomes self diagnostic mode when this terminal is Low and power switch is turned on.
18, 19	PC7, NMI	-	-	Not used
20	INT1	INT1	In	Interrupt from the gate array
21	MODE1	-	-	Not used
22	RESET	-	In	Power ON reset signal input
23	MODE0	-	-	Not used
24, 25	X2, X1	-	In/Out	15M Hz clock pulse input/output
26	VSS	-	-	Ground (0 V) source
27	AVSS	-	-	Ground for the built-in ADCs
28	AN0	ENV1	In	Envelope signal from the 1st string
29	AN1	ENV2	In	Envelope signal from the 2nd string
30	AN2	ENV3	In	Envelope signal from the 3rd string
31	AN3	ENV4	In	Envelope signal from the 4th string
32	AN4	ENV5	In	Envelope signal from the 5th string
33	AN5	ENV6	In	Envelope signal from the 6th string
34, 35	AN6, AN7	-	-	Not used
36	VREF	-	In	Reference voltage (+5 V) for the built-in ADCs
37	AVDD	-	In	+5 V source for built-in ADCs

38	$\overline{\text{RD}}$	R	Out	Memory read signal
39	$\overline{\text{WR}}$		Out	Memory write signal
40	ALE	-	Out	Address Latch Enable. Data bus PDO - PD7 become lower address (A0-A7) bus.
41 - 48	PF0-PF7	-	Out	Upper address (A8 - A15) bus
49 - 56	PDO-PD7	-	In/out	Data bus
57	STOP	-	-	Not used
58	VDD	-	-	+5 V source

F GATE ARRAY F

The gate array contains counters which detects the frequency of string vibration, an address latch, and a MIDI data buffer. The following is the pin function of the gate array.

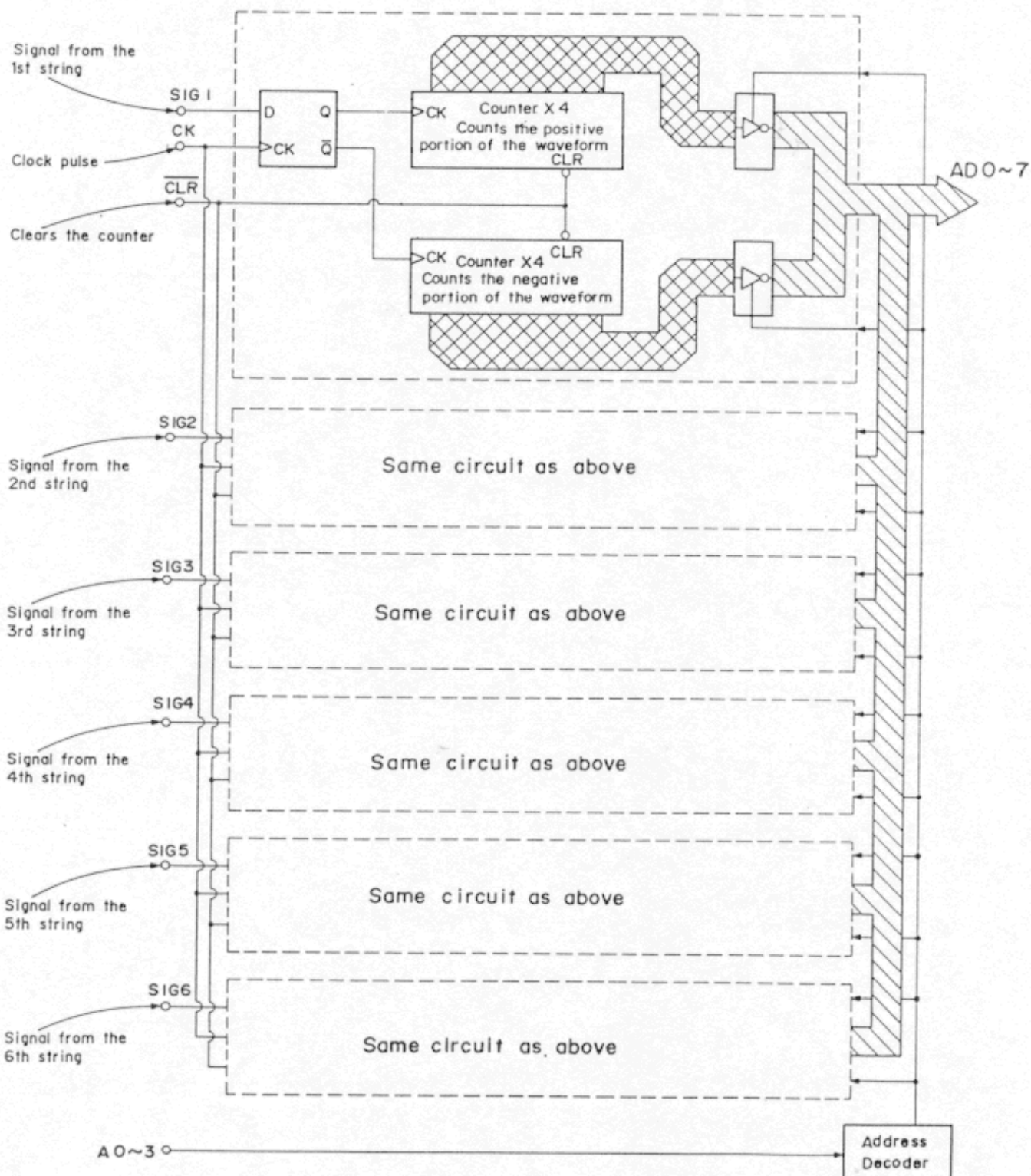
Pin No.	Terminal	Signal	In/Out	Function
1 - 10	AD0-AD7	AD0-AD7	In/Out	Data bus
3, 7	GND	DG	-	Ground (0 V) source
11 - 20	A0-A7	A0-A7	Out	Lower address bus
12, 23	CS2, CS1	A15, A14	In	Built-in counter provides frequency data from data bus when this terminal is Low and terminal CS1 is High
21	VDD1	VDD	-	+5 V source
22	ALE	ALE	In	Address Latch Enable signal. When this terminal is High, the contents of data bus are latched and become lower address bus (A0 - A7).
24	$\overline{\text{WR}}$	$\overline{\text{WR}}$	In	When Low, peak signals from the strings cannot be entered.
25	VDD2	VDD	-	+5 V source
26	$\overline{\text{RD}}$	$\overline{\text{RD}}$	In	When Low, note number is provided in data bus.
27	P1	PEAK 1	In	1st string's peak signal input
28	S1	SIG 1	In	1st string's frequency signal input
29	P2	PEAK 2	In	2nd string's peak signal input
30	S2	SIG 2	In	2nd string's frequency signal input
31	P3	PEAK 3	In	3rd string's peak signal input
32	S3	SIG 3	In	3rd string's frequency signal input
33	GND	DG	-	Ground (0 V) source
34	VDD	VDD	In	+5 V source
35	P4	PEAK 4	In	4th string's peak signal input
36	S4	SIG 4	In	4th string's frequency signal input

37	P5	PEAK 5	In	5th string's peak signal input
38	S5	SIG 5	In	5th string's frequency signal input
39	P6	PEAK 6	In	6th string's peak signal input
40	S6	SIG 6	In	6th string's frequency signal input
41 - 45	-	-	-	Not used
46	M0	M0	Out	MIDI data output
47	$\overline{\text{CLR}}$	$\overline{\text{CLR}}$	In	Frequency detection counter reset signal
48	MI	MI	In	MIDI data input
49	CK	CLK	In	Clock pulse for frequency detection counter
50	INT1	INT1	Out	Interrupt to CPU
51, 52	-	-	-	Not used

6 INTERNAL CIRCUITS OF GATE ARRAY F

(1) Frequency Detection Counter

In order to detect the frequency of strings' vibrations, sexadecimal counter in Gate Array F counts up the positive and negative portions of the waveform from the strings, and provides digital data to CPU via data bus.

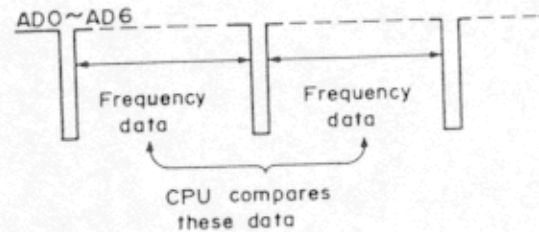


(2) Peak Detection Circuit

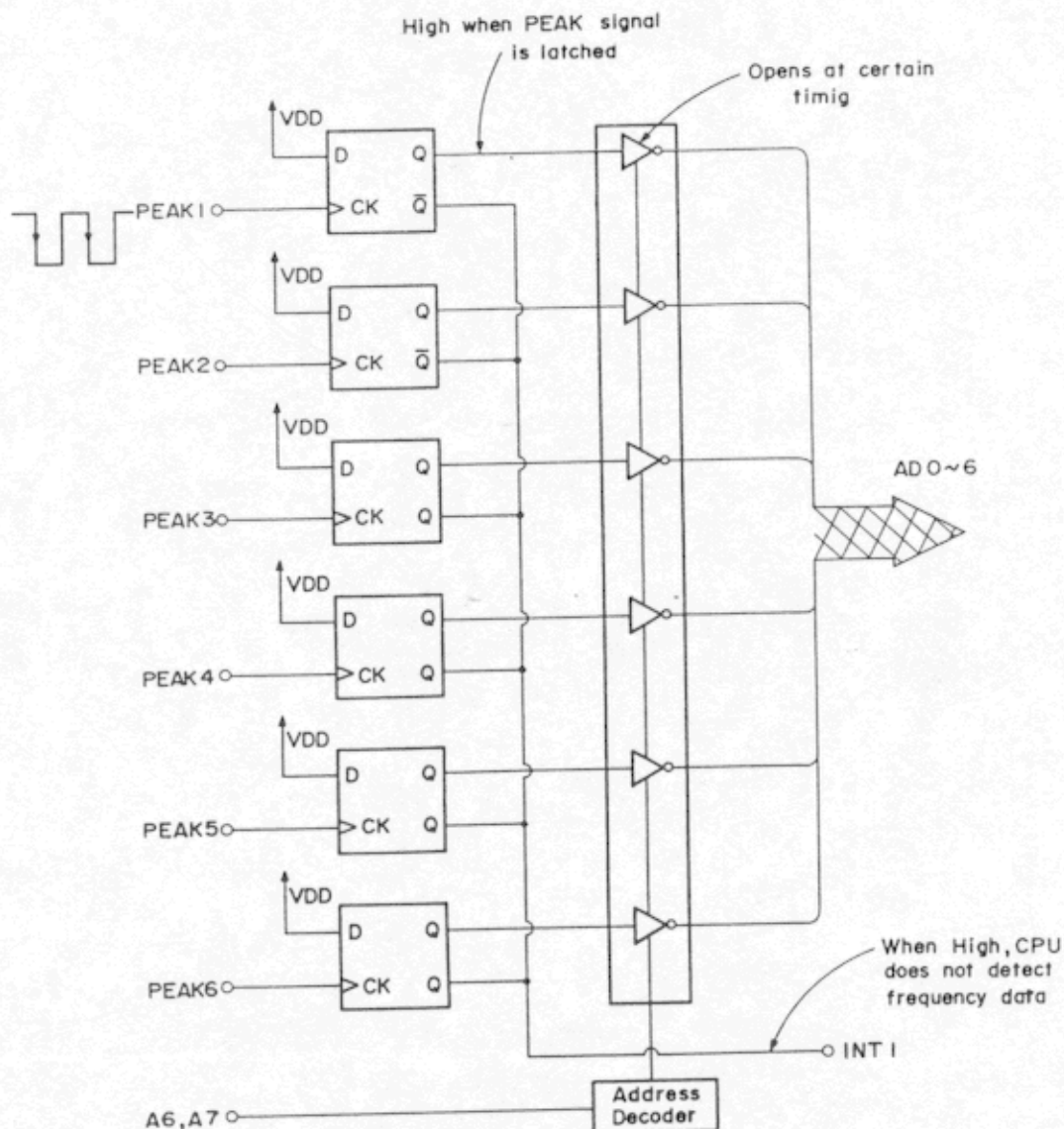
The circuit disregards abnormal string vibration which may occur at the beginning and the end of string vibration and detects the accurate frequency of string vibrations.

PEAK signals are provided at the peaks of string vibration waveform and latched in the flip flops. While a PEAK signal is latched, output Q of the flip flop rises to High level.

At certain timing, CPU opens the tri-state inverters by signals A6 and A7 so that data bus drop to Low. CPU receives frequency data from the counters between the period of being Low of AD0 - AD6. Every time CPU receives data, it compares the frequency with the formerly detected data and if there is a difference between the two data, CPU disregards the former data in order to detect the accurate frequency.

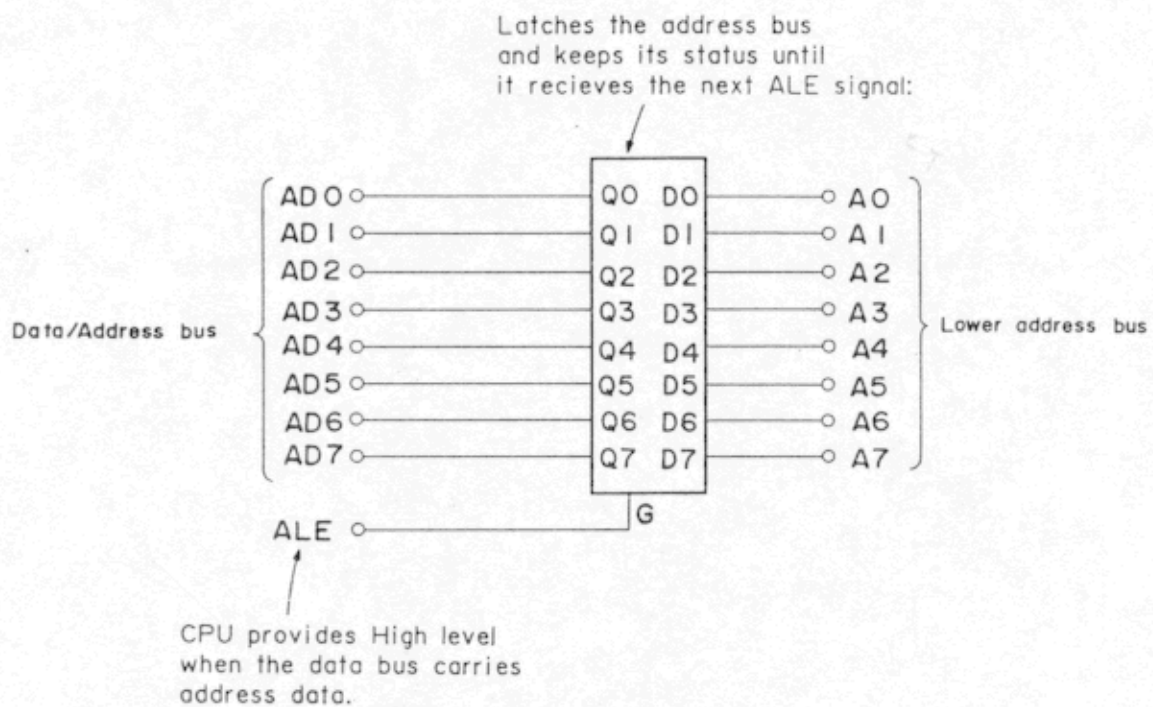


When PEAK signals are not provided, Q outputs of the flip flops interrupt the CPU via INT 1 terminal. Receiving INT 1, CPU stops detecting frequency data.



(3) Address Latch

Receiving signal ALE from CPU, signals AD0 - AD7 are latched in and become lower address signals A0 - A7.



(4) MIDI Buffer

Amplifies the MIDI output signal from CPU.

